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MODELING OF THE I–V CHARACTERISTICS FOR LDD-nMOSFETs IN RELATION WITH DEFECTS INDUCED BY HOT-CARRIER INJECTION

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The hot-carrier injection is observed increasingly to degrade the I–V characteristics with the scaling of MOS transistors. For the lightly doped drain MOS transistor the injection of the hot-carriers, caused by the high electric field in the MOS structure, is localized in the LDD region. The modeling of the drain current in relation to defects due to the hot-carrier injection allows us to investigate the I–V characteristics and the transconductance of devices. Consequently, we can know the amount of the device degradation caused by these defects in order to find technological solutions to optimize reliability.

Keywords: I–V characteristics; MOS; LDD; Modeling; Defects

1 INTRODUCTION

One of the major problems that pose a serious constraint when reducing the channel length of the MOS transistor is the hot-carrier caused by the high electric field in the device structure. In order to reduce the hot-carrier effect, the LDD structure is used [1–3]. In this structure, the electric field maximum is reduced and is spread out in the n-region. However, hot-carriers are generated by impact ionization in the n-region under the sidewall spacer [4–5]. This leads to the reduction of the free carrier mobility and to the increase of the parasitic LDD resistance [6–8]. Understanding the physics of hot-carrier effects in silicon MOSFETs plays an important role in determining device degradation mechanisms and thus the improvement of MOSFET design. So to study the effect of these defects on the device reliability, it is very important to carry out a modeling of the I–V characteristics in relation to defects localized in the LDD region. Simulations of their evolutions allow us to know the amount of device degradation caused by these defects to find technological solutions in order to minimize the aging phenomenon of the transistor.

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2 MODELING OF THE DRAIN CURRENT

The defect density localized in the LDD region is represented by a Gaussian distribution, centered in the LDD region (Fig. 1) and expressed by:

$$N_{it}(y) = N_{it_{max}} \exp\left(\frac{-(y - y_c)^2}{2\sigma^2}\right) \tag{1}$$

where $N_{it_{max}}$, y_c and σ are the maximum, the center and the standard deviation of the Gaussian distribution.

2.1 Linear Regime

The source-drain voltage V_{DS} is expressed, in the linear regime as:

$$V_{DS} = V_{D_1S_1} + V_{D_2D_1} + V_{D_3D_2} + I_{DS}(R_S + R_D) \tag{2}$$

where $V_{D_1S_1}, V_{D_2D_1}, V_{D_3D_2}$ are, respectively, the dropped potentials in intrinsic, overlapped and non-overlapped regions. R_S and R_D are the source and drain resistances.

In the intrinsic region the drain current can be expressed as [9]:

$$I_{DS} = \frac{\bar{\mu}_s W C_{ox}[V_{GS} - V_{T_0} + \Delta V_T - \overline{\Delta V_{FB}} - (F_B/2)V_{D_1S_1}]V_{D_1S_1}}{L + (V_{D_1S_1}/\overline{E_{sat}}) + \bar{\mu}_s W C_{ox} R_S F_B V_{D_1S_1}} \tag{3}$$

where:

$$\begin{cases} V_{T_0} = V_{FB} + 2\phi_f + \gamma\sqrt{2\phi_f + V_{SB}} \\ F_B = \dfrac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} + 1 \\ \gamma = \dfrac{\sqrt{2q\varepsilon_S N_A}}{C_{ox}} \\ \Delta V_T = \dfrac{1}{k^2}\dfrac{\partial^2 V(y)}{\partial y^2} \end{cases}$$

where μ_s, W, C_{ox} and V_{GS} are, respectively, the surface mobility, the channel width, the gate oxide capacitance per unit area and the gate bias. V_{T_0} is the threshold voltage and ΔV_T

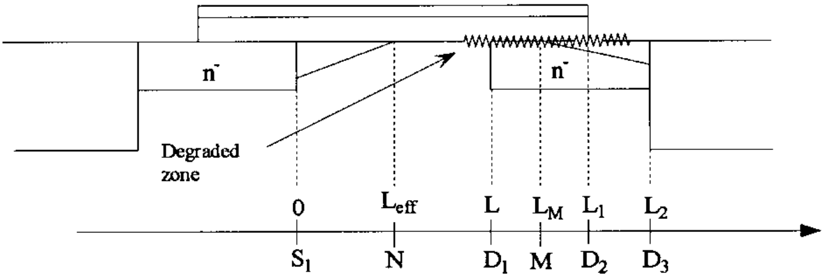

FIGURE 1 Schematic diagram of LDD MOSFET with localized defects.

represents the threshold voltage reduction caused by the lateral electric field, which is very weak in the linear regime that we can consider it as constant.

$$\begin{cases} \overline{\Delta V_{FB}} = \dfrac{q\overline{N_{it}(y)}}{C_{ox}} \\ \overline{\mu_s} = \dfrac{\mu_0}{[1+\theta(V_{GS}-V_{T_0})][1+\beta\overline{N_{it}(y)}]} \\ \overline{E_{sat}} = \dfrac{2\vartheta_{sat}}{\mu_0}[1+\theta(V_{GS}-V_{T_0})][1+\beta\overline{N_{it}(y)}]. \end{cases} \tag{4}$$

θ and β are the fitting parameters. The spatial average of the defect density $\overline{N_{it}(y)}$ is expressed as:

$$\overline{N_{it}(y)} = \sqrt{\frac{\pi}{2}}\frac{N_{it_{max}}\sigma}{L}\left[\mathrm{erf}\left(\frac{L-y_c}{\sqrt{2}\sigma}\right)+\mathrm{erf}\left(\frac{y_c}{\sqrt{2}\sigma}\right)\right]. \tag{5}$$

From Eq. (3) we derive $V_{D_1S_1}$:

$$V_{D_1S_1} = \frac{-V_2-\sqrt{V_2^2-4V_1V_3}}{2V_1} \tag{6}$$

where:

$$\begin{cases} V_1 = \dfrac{\bar{\mu}F_BWC_{ox}}{2} \\ V_2 = \dfrac{I_{DS}}{\overline{\overline{E_{sat}}}} - \bar{\mu}WC_{ox}[V_{GS}-V_{T_0}+\Delta V_T-\overline{\Delta V_{FB}}-F_BR_sI_{DS}] \\ V_3 = I_{DS}L. \end{cases}$$

The drain current at the overlapped-LDD region is expressed by:

$$I_{DS} = \frac{W\bar{\mu}_sC_{ox}[(V_{GS}-V_{T_n}+\Delta V_T-\overline{\Delta V_{FB}})-F_{B_n}((V_{D_2D_1}/2)+V_{D_1S_1})]V_{D_2D_1}}{(L_1-L)[1+(W\bar{\mu}_sC_{ox}F_{B_n}R_SV_{D_2D_1})/(L_1-L)+V_{D_2D_1}/\overline{E_{sat}}(L_1-L)]}. \tag{7}$$

From this equation we can obtain $V_{D_2D_1}$ as:

$$V_{D_2D_1} = \frac{U_2-\sqrt{U_2-4U_1U_3}}{2U_1} \tag{8}$$

$$\begin{cases} U_1 = \dfrac{\bar{\mu}_sF_{B_n}WC_{ox}}{2} \\ U_2 = I_{DS}\left[W\bar{\mu}_sC_{ox}R_sF_{B_n}+\dfrac{1}{\overline{\overline{E_{sat}}}}\right] - \bar{\mu}_sWC_{ox}[V_{GS}-V_{T_n}+\Delta V_T-\overline{\Delta V_{FB}}-F_{B_n}V_{D_1S_1}] \\ U_3 = I_{DS}(L_1-L). \end{cases}$$

Using a similar method effectuated in the overlapped region, we derive the following expression for the drain:

$$I_{DS} = \frac{W\bar{\mu}_s\bar{C}_{ox}[(V_{GS}-\bar{V}_{T_n}+\Delta V_T-\overline{\Delta V_{FB}})-\bar{F}_{B_n}((V_{D_3D_2}/2)+V_{D_2S_1})]V_{D_3D_2}}{(L_2-L_1)[1+(W\bar{\mu}_s\bar{C}_{ox}\bar{F}_{B_n}R_SV_{D_3D_2})/(L_2-L_1)+V_{D_3D_2}/\overline{E_{sat}}(L_2-L_1)]}. \tag{9}$$

Using expression (9) we obtain $V_{D_3D_2}$ as:

$$V_{D_3D_2} = \frac{U_2' - \sqrt{U_2' - 4U_1'U_3'}}{2U_1'} \tag{10}$$

$$\begin{cases} U_1' = \dfrac{\bar{\mu}_s \overline{F_{B_n}} W \overline{C_{ox}}}{2} \\ U_2' = I_{DS}\left[W \bar{\mu}_s \overline{C_{ox}} R_s \overline{F_{B_n}} + \dfrac{1}{\overline{E_{sat}}}\right] - \bar{\mu}_s W \overline{C_{ox}} [V_{GS} - \overline{V_{T_n}} + \Delta V_{T_n} - \overline{\Delta V_{FB}} - \overline{F_{B_n}} V_{D_2S_1}] \\ U_3' = I_{DS}(L_2 - L_1). \end{cases}$$

The drain current in the linear regime is obtained by substituting $V_{D_1S_1}, V_{D_2D_1}$ and $V_{D_3D_2}$ in Eq. (2).

2.2 Saturation Regime

When V_{DS} becomes greater than the saturation voltage, the depleted zones in the intrinsic and LDD region increase (Fig. 1). In this case V_{DS} is written as:

$$V_{DS} = V_{MS_1} + V_{D_2M} + V_{D_3D_2} + I_{DS}(R_S + R_D). \tag{11}$$

$V_{D_3D_2}$ is given by the expression (10) and V_{D_2M} is obtained by replacing L by L_M in Eq. (8). Calculating V_{MS_1} gives the drain current in the saturation regime.

In the saturation region $N < y < D_1$, the value of the lateral electric field becomes more important and ΔV_T cannot be regarded as a constant. From Eq. (3) we obtain the following differential:

$$\frac{\partial^2 V_{CS_1}}{\partial y^2} - p^2 V_{CS_1} = p^2\left[I_{DS}\frac{1 + f R_S}{f} - \frac{V_{GS} - V_{T_0} + \Delta V_{FB}}{F_B}\right] \tag{12}$$

where:

$$\begin{cases} p^2 = F_B k^2 \\ f = W C_{ox} \vartheta_{sat} F_B. \end{cases}$$

The boundary conditions at the pinch-off point (point N) are: $V_{CS_1}(y = L_{eff}) = V_{dsat}$ and $\frac{dV_{CS_1}}{dy}\Big|_{y=L_{eff}} = E_{sat}$. Using these boundary conditions the resolution of Eq. (12) gives the potential along the channel in the saturation mode:

$$\begin{aligned} V_{CS_1}(y) = {} & V_{dsat} + \frac{E_{sat}}{p}\sinh(p(y - L_{eff})) \\ & + \left[I_{DS}\frac{1 + f R_S}{f} - \frac{V_{GS} - V_{T_0}}{F_B} + V_{dsat}\right][\cosh(p(y - L_{eff})) - 1] \\ & - p\int_{L_{eff}}^{y} \frac{\Delta V_{FB}(y')}{F_B}\sinh(p(y' - y))\,dy'. \end{aligned} \tag{13}$$

The saturation regime also leads to the creation of a depleted zone in the LDD region. In the same way that in the case of the intrinsic region, the overlapped zone can be divided into two regions. In the first region ($M < y < D_2$) the variation of ΔV_{T_n} is weak whereas in the second region ($D_1 < y < M$) and cannot be regarded as a constant.

In the saturation region the canal potential is governed by the following differential equation:

$$\frac{\partial V_{CS_1}}{\partial y^2} - p_n^2 V_{CS_1} = p_n^2\left[I_{DS}\frac{1+f_nR_S}{f_n} - \frac{V_{GS}-V_{T_n}+\Delta V_{FB}}{F_{B_n}}\right] \tag{14}$$

$$\begin{cases} p_n^2 = \dfrac{F_{B_n}C_{ox}}{\varepsilon_s x_{dn}} \\ f_n = WC_{ox}\vartheta_{sat}F_{B_n}. \end{cases}$$

The boundary conditions at substrate-LDD junction are given by: $V_{CS_1}(y = L) = V_L$ and $\frac{dV_{CS_1}}{dy}\Big|_{y=L} = E_L$. V_L and E_L are determined using expression (13). Using the boundary conditions, the resolution of Eq. (14) gives the channel potential in the saturation region:

$$\begin{aligned} V_{CS_1}(y) = {} & V_L + \frac{E_L}{p_n}\sinh(p_n(y-L)) \\ & + \left[I_{DS}\frac{1+f_nR_S}{f_n} - \frac{V_{GS}-V_{T_0}}{F_{B_n}} + V_L\right][\cosh(p_n(y-L))-1] \\ & - p_n\int_L^y \frac{\Delta V_{FB}(y')}{F_{B_n}}\sinh(p_n(y'-y))\,dy' \end{aligned} \tag{15}$$

at the point M we have: $V_{CS_1}(y = L_M) = V_{MS_1}$ and $E(y = L_M) = E_{sat}$. From these boundary conditions, one can obtain L_M and V_{MS_1}. Thus, the drain current in the saturation regime is obtained by substituting V_{MS_1}, V_{D_2M} and $V_{D_3D_2}$ in Eq. (11).

3 SIMULATION RESULTS

The parameters of the transistor used in the simulation are given in Table I.

3.1 Defects Influence on the I_{DS}–V_{DS} Characteristic

The curves of Figures 2a and 2b show the influence of the defects on characteristic I_{DS}–V_{DS}. The presence of the defect density localized in the LDD region involves a reduction of the current drain. This reduction is accentuated with the increase of the maximum of the defect density (Figure 2a). The extension of the degraded zone also leads to the degradation of the current drain (Figure 2b). In the saturation mode part, the interface states are in the velocity saturation region and can be depleted, therefore the effect of these interface states becomes insignificant.

TABLE I Transistor Parameters Used in Simulations.

Parameters	Values
L/W	0.7 µm/1 µm
$L_1 - L/L_2 - L$	0.15 µm/0.25 µm
T_{ox} /NA	20 nm/2.3 × 10^{16} cm^{-3}
θ/β	0.18 µm/2.5 × 10^{-12}
μ_0/ϑ_{sat}	600 cm^{2}V^{-1}s^{-1}/7 × 10^6 cm s^{-1}

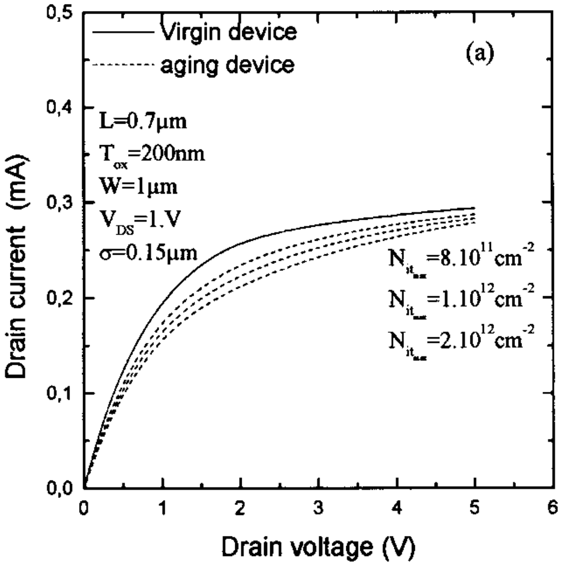

FIGURE 2a I–V characteristics evolution with defect density maximum variation.

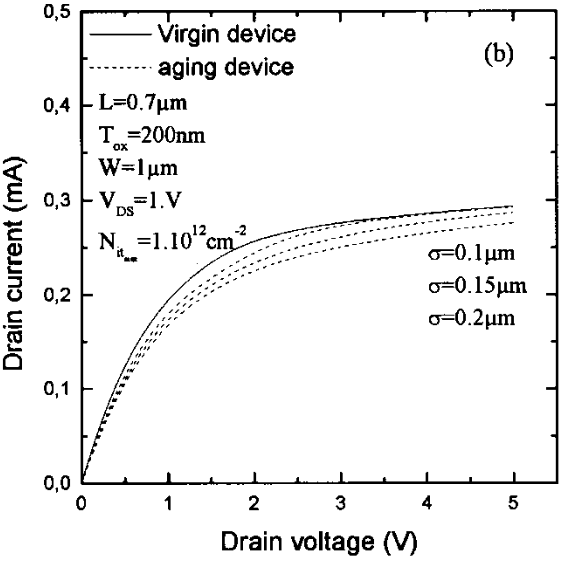

FIGURE 2b Impact of the degraded zone extension on I–V characteristics.

3.2 Defects Influence on the Transconductance

The curves of Figure 3a represent the evolution of the transconductance according to the gate bias for various densities of interface defects localized in the LDD region. Simulations show that the transconductance decreases when the defect density increases. This transconductance degradation is reduced as the gate voltage increases. Indeed, when the gate voltage increases,

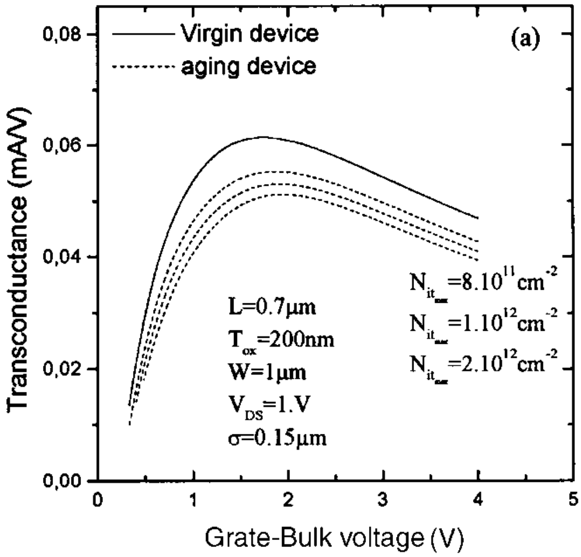

FIGURE 3a Influence of the variation, of the defect density maximum on the transconductance.

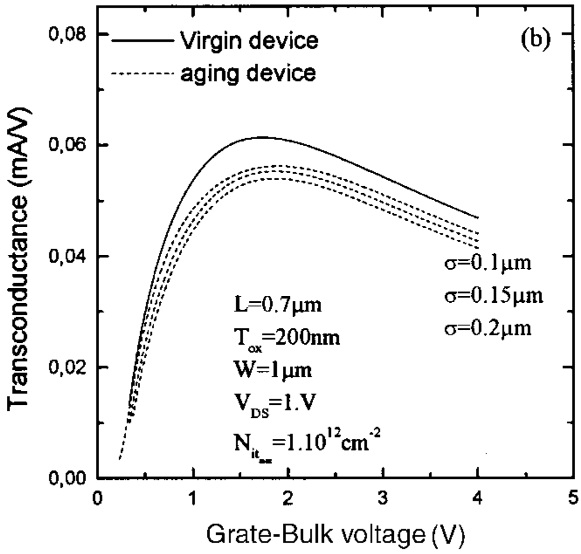

FIGURE 3b Transconductance variation versus gate bias for different degraded zone extensions.

the carrier density in the inversion layer increases and the effects of Coulomb scattering are reduced by the screening effect. Thus, the degradation of transconductance is less significant. We have also represented in Figure 3b the effect of the increase of the degraded zone on the transconductance. The extension of the damaged zone also leads to the transconductance degradation.

4 CONCLUSION

The modeling of the drain current for a lightly doped drain MOSFET in relation to defects localized in the LDD region is very important. It allows us to understand the aging phenomenon and the amount degradation of the performances of the devices. The simulation results show that the stress leads to the degradation of the I–V characteristic and the reduction of the transconductance. The model can be applied to the simulation of device behavior after stress in order to improve the long-term circuit reliability.

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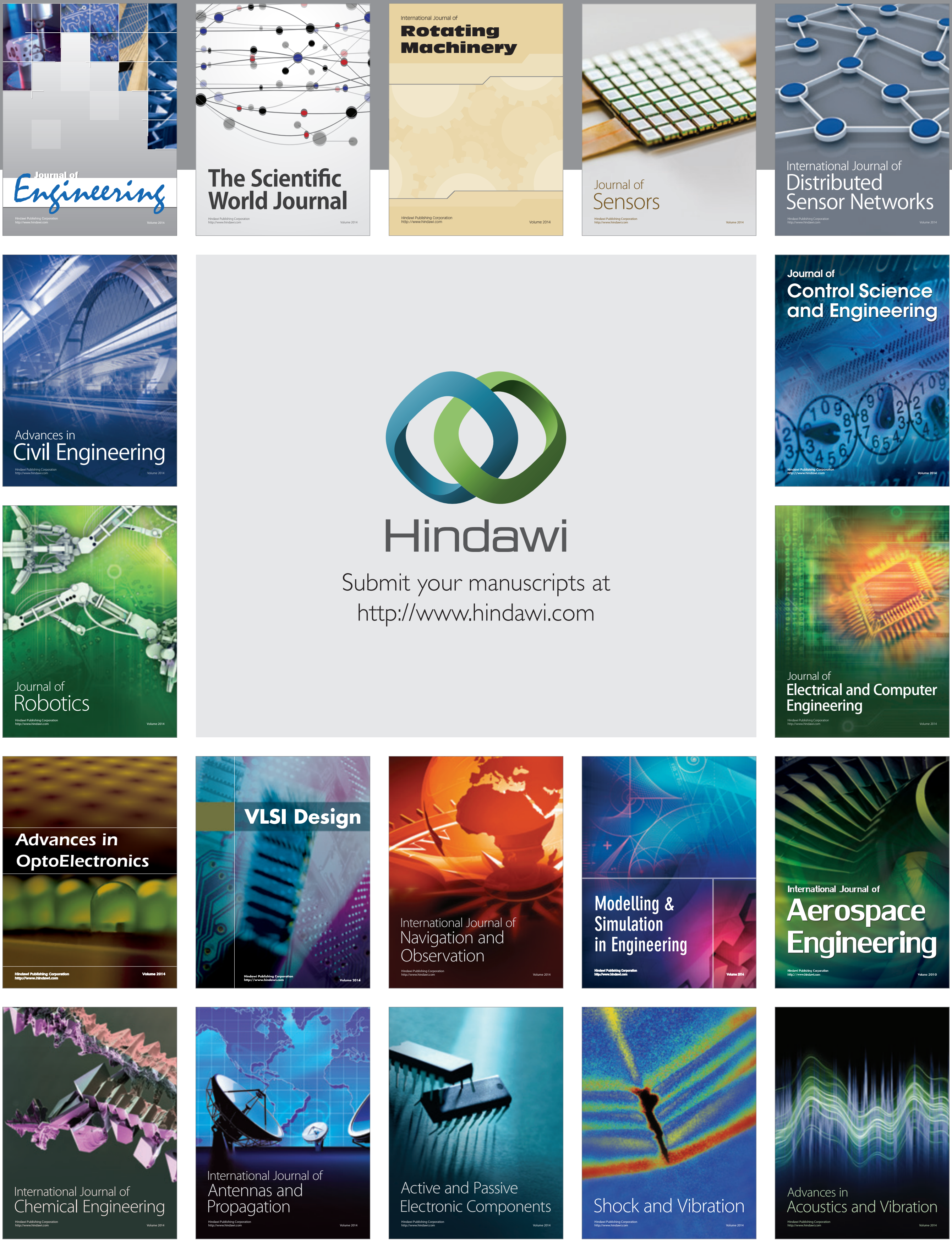
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